100G 100m CFP Optical Transceiver, Hot Pluggable MPO/MTP, +3.3V, VCSEL & PIN, Multi mode

Features:

- ✧ Compliant to IEEE 802.3ba 100GBASE SR10
- ✧ 10 independent full-duplex channels
- ✧ Aggregate bandwidth of > 100Gbps
- ✧ Form factors compliant to CFP MSA
- ✧ CAUI high speed electrical interface
- ✧ IEEE compliant MDIO interface for management and digital diagnostic monitor
- ✧ Transmission data rate up to 11.18 Gbit/s per channel
- ✧ Power class 1 (< 7W max)
- ✧ 10 channels 850nm VCSEL array transmitter
- ✧ 10 channels PIN photo detector array receiver
- ✧ Capable of over 100 m transmission on high bandwidth 50μm multi-mode ribbon fiber
- ✧ Single +3.3V power supply, operating case temperature: 0~70℃
- ✧ All-metal housing for superior EMI Performance
- ✧ RoHS compliant
- ✧ No reference clock needed
- ✧ TX input and RX output CDR retiming
- ✧ Utilizes a standard 24/20 lane optical fiber with MPO connector
- ✧ OTU4 compatible

Applications:

- ✧ Rack torack
- ✧ Data centers
- ✧ Metro networks
- ✧ Switches and Routers

Description:

The CFP optical transceiver module are a high performance, low power consumption, short reach(1m to100m) interconnect solution supporting 100G Ethernet and Telecom. It is compliant with the CFP MSA and IEEE P802.3ba 100GBASE-SR10. The CFP SR10 modules offer 10 transmit and 10 receive asynchronous channels operating at up to 11.18Gbps per channel.

As shown in Figure 1, the transmitter side of the module consists of an array of VCSELs (Vertical Cavity Surface Emitting Lasers) and associated circuitry, which converts 10 parallel electrical data inputs to 10 parallel optical data output signals and also converts 10 parallel optical signals into 10 parallel electrical signals through an array of PIN photodiodes and associated circuitry.

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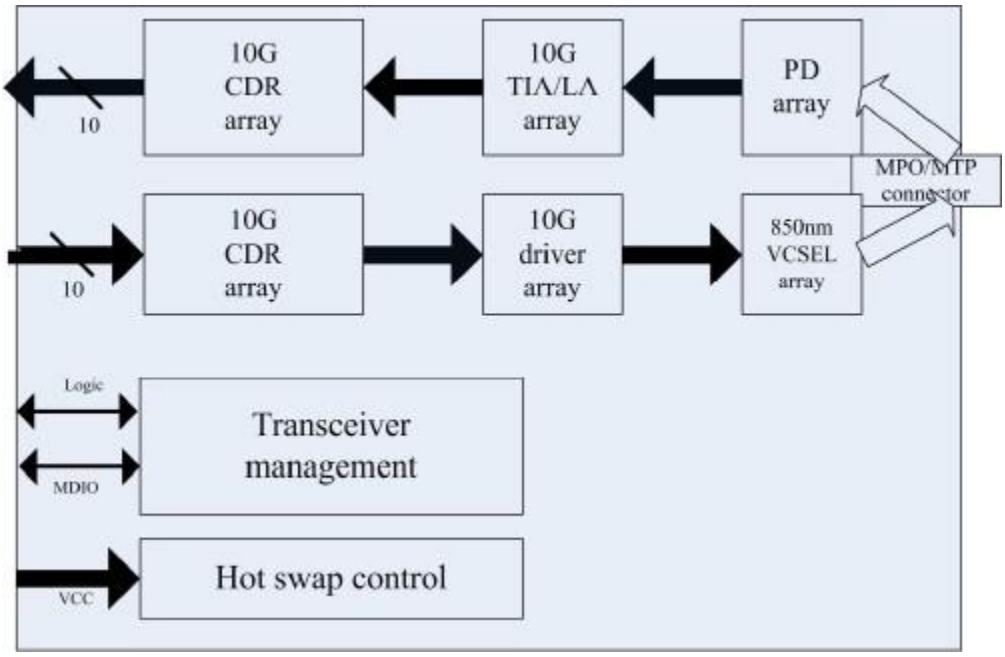

Figure1.Module Block Diagram

● Absolute Maximum Ratings

Parame ter	Symbol	Min	Max	Unit
Supply	Voltage	Vcc	-0.5	3.6
Input	Voltage	Vin	-0.3	Vcc+0.3
Storage	Temperature	Tst	-40	85
Humidity(non-condensing)	Rh	5	85	%

***Exceeding any one of these values may destroy the device immediately**

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Supply	Voltage	Vcc	3.13	3.3	3.47
Operating	Case	temperature	Tca	0	70
Data	Rate	Per	Lane	fd	-
Power	Dissipation	Pm	7	W	
Low	Power	Mode	Dissipation	Plow	2
Aggregate	Bit	Rate	BRaggr	103.125	111.8

● Electrical Characteristics

Parame ter	Symbol	Min	Typical	Max	Unit	
Differential input impedance	Zin	90	100	110	Ω	
Differential input impedance	Zout	90	100	110	Ω	
Differential input voltage amplitude	Δ Vin	120		820	mVp-p	
Differential output voltage amplitude	Δ Vout	300		820	mVp-p	
Input Logic Level High	VIH	2.0		Vcc+0.3	V	3.3V LVCOMS
		0.84		1.2		1.2V LVCOMS
Input Logic Level Low	VIL	-0.3		0.8	V	3.3V LVCOMS
		-0.3		0.36		1.2V LVCOMS

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Output Logic Level High	VOH	Vcc-0.2		Vcc	V	3.3V LVCOMS
		1.0		1.5		1.2V LVCOMS
Output Logic Level Low	VOL	0		0.2	V	3.3V LVCOMS
		-0.3		0.2		1.2V LVCOMS

Note:
1. Differential input voltage amplitude is measured between TxnP and TxnN.
2. Differential output voltage amplitude is measured between RxnP and RxnN.

● Optical Characteristics (T = 25° C, VCC =3.3V +/- 5%)

Parameter	Symbol	Min	Typical	Max	Unit
Transmitte r Optical Specifications (T = 25°C, VCC =3.3V +/- 5%)					
Average optical power(per channel)	Pout	-7.6	-1	+2.4	dBm
Average(per channel) - disabled	Poff			-30	dBm
Optical return loss tolerance				12	dB
Extinction ratio	ER	3			dB
Center wavelength	λc	840	850	860	nm
RMS spectral width	λ		0.5	0.65	nm
Transmit OMA, per lane	TX_OMA/lane	-5.6		3	dBm
Difference in launch power between any two lanes(OMA)				4	dB
Transmitter and dispersion penalty, each lane	TDP/lane			3.5	dB
Transmitter eye mask	Compliant to IEEE802.3ba eye mask specification				
Receiver Optical Specifications (T = 25° C, VCC =3.3V +/- 5%)					
Optical power sensitivity (per channel)	Pin min	-	-12	-9.9	dBm
Optical power saturation (per channel)	Pin max	+1	-	-	dBm
Stressed receiver sensivity	Ps	-	-	-5.4	dBm
Center wavelength	λc	840	850	860	nm
RMS spectral width	λ		0.5	0.65	nm
Optical return loss	RI	12			dB
Damage threshold		3.4			dBm
Optical modulation amplitude, each lane				3	dBm

Note:
1. Average optical power is measured at the output of the modules optical interface.
2. Optical power sensitivity is measured with BER@10^{-12} at 10.3125Gbps per channel.

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CFP module functional block diagram

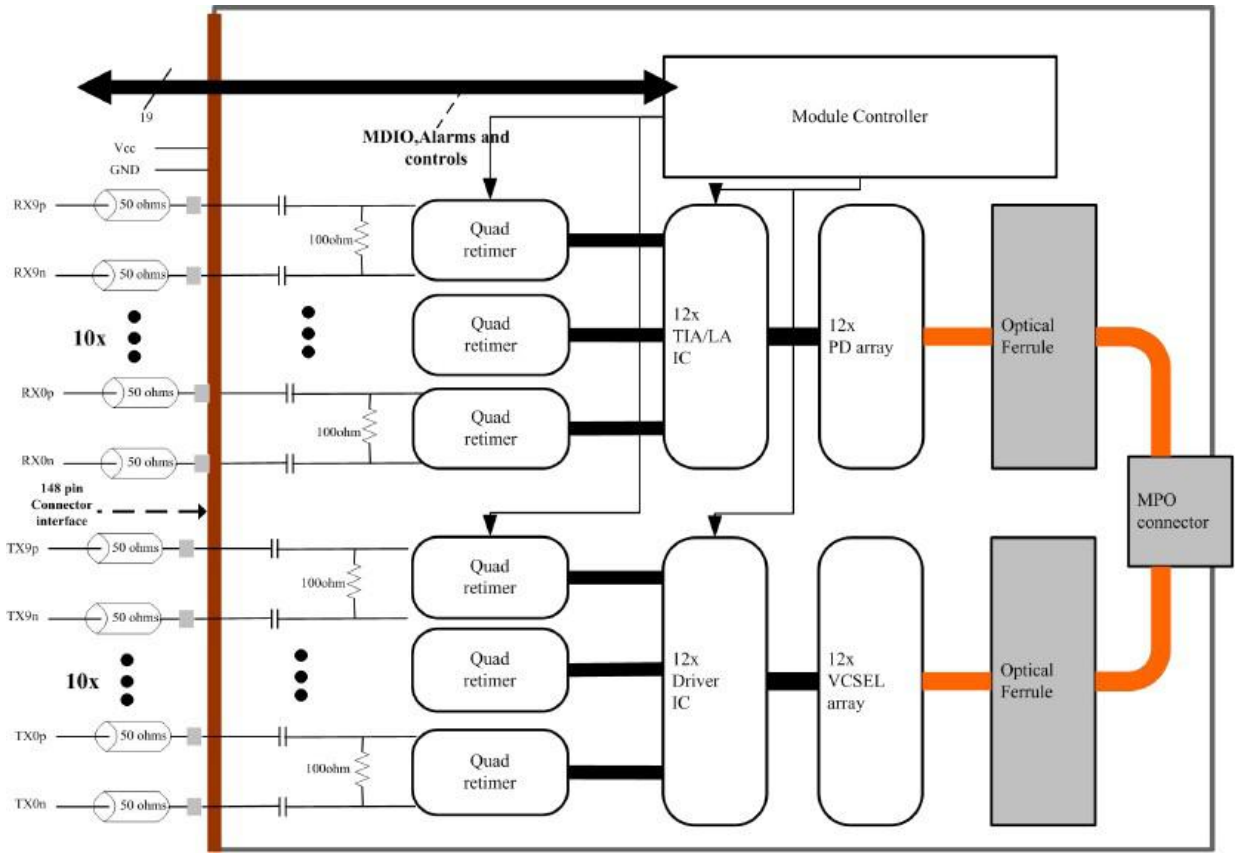

Figure 2. CFP module functional block diagram

Pin Description:

- **Part 1:Bottom Row Pin Function Definition**

PIN	Name	I/O	Logic	Description
1	3.3V_GND			3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground
2	3.3V_GND			
3	3.3V_GND			
4	3.3V_GND			
5	3.3V_GND			
6	3.3V			3.3V Module Supply Voltage
7	3.3V			
8	3.3V			
9	3.3V			
10	3.3V			
11	3.3V			
12	3.3V			
13	3.3V			
14	3.3V			
15	3.3V			

16	3.3V_GND			3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground
17	3.3V_GND			
18	3.3V_GND			
19	3.3V_GND			
20	3.3V_GND			
21	VND_IO_A	I/O		Module Vendor I/O. Must No Connect at host board
22	VND_IO_B	I/O		Module Vendor I/O. Must No Connect at host board
23	GND			
24	TX_MCLKn	O	CML	For optical waveform testing. Not for normal use.
25	TX_MCLKp	O	CML	For optical waveform testing. Not for normal use.
26	GND			
27	VND_IO_C	I/O		Module Vendor I/O. Must No Connect at host board
28	VND_IO_D	I/O		Module Vendor I/O. Must No Connect at host board
29	VND_IO_E	I/O		Module Vendor I/O. Must No Connect at host board
30	PRG_CNTL1	I	LV CMOS w/ PUR	Programmable Control 1 set over MDIO, MSA Default: TRXIC_RSTn, TX & RX ICs reset, "0": reset, "1" or NC: enabled = not used
31	PRG_CNTL2	I	LV CMOS w/ PUR	Programmable Control 2 set over MDIO, MSA Default: Hardware Interlock LSB, "00": ≤8W, "01":≤16W, "10": ≤24W, "11" or NC: ≤32W = not used
32	PRG_CNTL3	I	LV CMOS w/ PUR	Programmable Control 3 set over MDIO, MSA Default: Hardware Interlock MSB, "00": ≤8W, "01": ≤16W, "10": ≤24W, "11" or NC: ≤32W = not used
33	PRG_ALRM1	O	LV CMOS	Programmable Alarm 1 set over MDIO, MSA Default：RXS, RX CDR Lock Indicator, "1"：loss of lock, "0"：locked
34	PRG_ALRM2	O	LV CMOS	Programmable Alarm 2 set over MDIO, MSA Default: HIPWR_ON,, "1": module power up completed, "0"：module not powered up
35	PRG_ALRM3	O	LV CMOS	Programmable Alarm 3 set over MDIO, MSA Default: MOD_READY, initialization sequence done, "1": done, "0": not done
36	TX_DIS	I	LV CMOS	Transmitter Disable for all lanes, "1" or NC = transmitter disabled, "0" = transmitter enabled
37	MOD_LOPWR	I	LV CMOS w/ PUR	Module Low Power Mode. "1" or NC: module in low power (safe) mode, "0": power-on enabled
38	MOD_ABS	O	GND	Module Absent. "1" or NC: module absent, "0":module present, Pull Up Resistor on Host
39	MOD_RSTn	I	LV CMOS w/ PDR	Module Reset. "0" resets the module, "1" or NC = module enabled, 4.75kohm Pull Down Resistor in Module

40	RX_LOS	O	LV CMOS	Receiver Loss of Optical Signal, "1"：low optical signal, "0"：normal condition
41	GLB_ALRMn	O	LV CMOS	Global Alarm. “0"：alarm condition in any MDIO Alarm register, "1"：no alarm condition
42	PRTADR4	I	1.2V	MDIO Physical Port address bit 4
43	PRTADR3	I	1.2V	MDIO Physical Port address bit 3
44	PRTADR2	I	1.2V	MDIO Physical Port address bit 2
45	PRTADR1	I	1.2V	MDIO Physical Port address bit 1
46	PRTADR0	I	1.2V	MDIO Physical Port address bit 0
47	MDIO	I/O	1.2V CMOS	Management Data I/O bi-directional data (electrical specs as per 802.3ae and ba)
48	MDC	I	1.2V CMOS	Management Data Clock (electrical specs as per 802.3ae and ba)
49	GND			
50	VND_IO_F	I/O		Module Vendor I/O. Must No Connect at host board
51	VND_IO_G	I/O		Module Vendor I/O. Must No Connect at host board
52	GND			
53	VND_IO_H	I/O		Module Vendor I/O. Must No Connect at host board
54	VND_IO_J	I/O		Module Vendor I/O. Must No Connect at host board
55	3.3V_GND			3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground
56	3.3V_GND			
57	3.3V_GND			
58	3.3V_GND			
59	3.3V_GND			
60	3.3V			3.3V Module Supply Voltage
61	3.3V			
62	3.3V			
63	3.3V			
64	3.3V			
65	3.3V			
66	3.3V			
67	3.3V			
68	3.3V			
69	3.3V			
70	3.3V_GND			3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground
71	3.3V_GND			
72	3.3V_GND			
73	3.3V_GND			
74	3.3V_GND			

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Part 2:Top Row Pin Function Definition

PIN	Name	I/O	Logic	Description
75	GND			
76	RX_MCLKp	O		RX Monitor Clock Output (Positive)
77	RX_MCLKn	O		RX Monitor Clock Output (Negative)
78	GND			
79	RX0p	O	HS I/O	Lane 0 Receiver Output (Positive)
80	RX0n	O	HS I/O	Lane 0 Receiver Output (Negative)
81	GND			
82	RX1p	O	HS I/O	Lane 1 Receiver Output (Positive)
83	RX1n	O	HS I/O	Lane 1 Receiver Output (Negative)
84	GND			
85	RX2p	O	HS I/O	Lane 2 Receiver Output (Positive)
86	RX2n	O	HS I/O	Lane 2 Receiver Output (Negative)
87	GND			
88	RX3p	O	HS I/O	Lane 3 Receiver Output (Positive)
89	RX3n	O	HS I/O	Lane 3 Receiver Output (Negative)
90	GND			
91	RX4p	O	HS I/O	Lane 4 Receiver Output (Positive)
92	RX4n	O	HS I/O	Lane 4 Receiver Output (Negative)
93	GND			
94	RX5p	O	HS I/O	Lane 5 Receiver Output (Positive)
95	RX5n	O	HS I/O	Lane 5 Receiver Output (Negative)
96	GND			
97	RX6p	O	HS I/O	Lane 6 Receiver Output (Positive)
98	RX6n	O	HS I/O	Lane 6 Receiver Output (Negative)
99	GND			
100	RX7p	O	HS I/O	Lane 7 Receiver Output (Positive)
101	RX7n	O	HS I/O	Lane 7 Receiver Output (Negative)
102	GND			
103	RX8p	O	HS I/O	Lane 8 Receiver Output (Positive)
104	RX8n	O	HS I/O	Lane 8 Receiver Output (Negative)
105	GND			
106	RX9p	O	HS I/O	Lane 9 Receiver Output (Positive)
107	RX9n	O	HS I/O	Lane 9 Receiver Output (Negative)
108	GND			
109	NC			Not Connected Internally
110	NC			Not Connected Internally
111	GND			
112	GND			

113	TX0p	I	HS I/O	Lane 0 Transmitter Input (Positive)
114	TX0n	I	HS I/O	Lane 0 Transmitter Input (Negative)
115	GND			
116	TX1p	I	HS I/O	Lane 1 Transmitter Input (Positive)
117	TX1n	I	HS I/O	Lane 1 Transmitter Input (Negative)
118	GND			
119	TX2p	I	HS I/O	Lane 2 Transmitter Input (Positive)
120	TX2n	I	HS I/O	Lane 2 Transmitter Input (Negative)
121	GND			
122	TX3p	I	HS I/O	Lane 3 Transmitter Input (Positive)
123	TX3n	I	HS I/O	Lane 3 Transmitter Input (Negative)
124	GND			
125	TX4p	I	HS I/O	Lane 4 Transmitter Input (Positive)
126	TX4n	I	HS I/O	Lane 4 Transmitter Input (Negative)
127	GND			
128	TX5p	I	HS I/O	Lane 5 Transmitter Input (Positive)
129	TX5n	I	HS I/O	Lane 5 Transmitter Input (Negative)
130	GND			
131	TX6p	I	HS I/O	Lane 6 Transmitter Input (Positive)
132	TX6n	I	HS I/O	Lane 6 Transmitter Input (Negative)
133	GND			
134	TX7p	I	HS I/O	Lane 7 Transmitter Input (Positive)
135	TX7n	I	HS I/O	Lane 7 Transmitter Input (Negative)
136	GND			
137	TX8p	I	HS I/O	Lane 8 Transmitter Input (Positive)
138	TX8n	I	HS I/O	Lane 8 Transmitter Input (Negative)
139	GND			
140	TX9p	I	HS I/O	Lane 9 Transmitter Input (Positive)
141	TX9n	I	HS I/O	Lane 9 Transmitter Input (Negative)
142	GND			
143	NC			Not Connected Internally
144	NC			Not Connected Internally
145	GND			
146	REFCLKp	I		Reference Clock Input (Positive)
147	REFCLKn	I		Reference Clock Input (Negative)
148	GND			

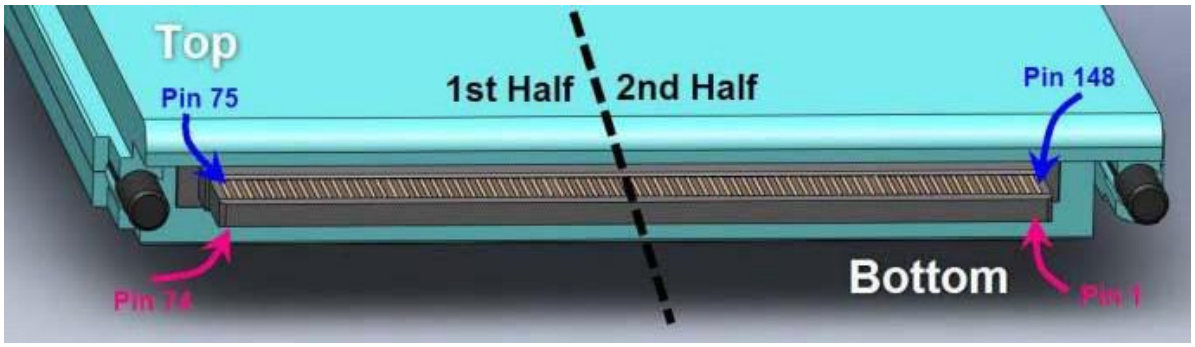


Figure3. Pad Layout of the CFP module

Optical Interface Lanes and Assignment

Figure 4 shows the orientation of the multi-mode fiber facets of the optical connector.

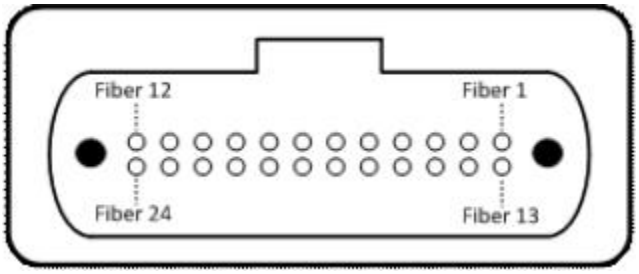


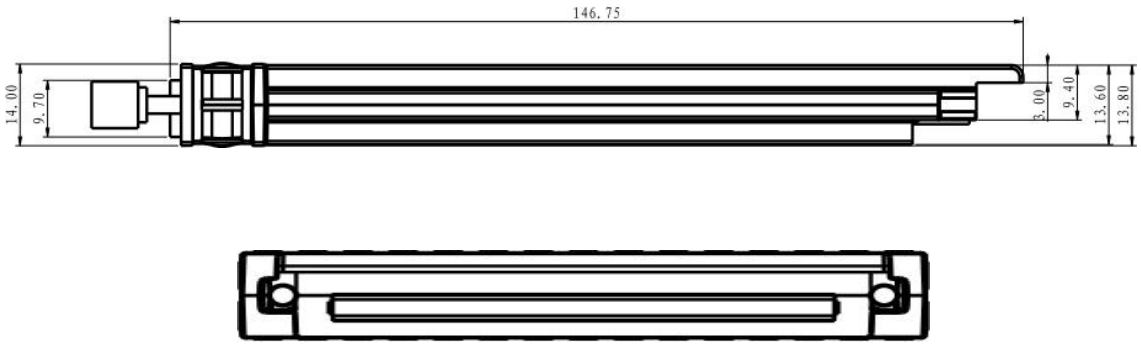
Figure 4: Outside view of the CFP module MPO receptacle

Fiber	Lane Assignment		Fiber #	Lane Assignment
1	Not		13	
2	RX0		14	TX0
3	RX1		15	TX1
4	RX2		16	TX2
5	RX3		17	TX3
6	RX4		18	TX4
7	RX5		19	TX5
8	RX6		20	TX6
9	RX7		21	TX7
10	RX8		22	TX8
11	RX9		23	TX9
12	Not used		24	Not used

Mechanical Dimensions:

100Gb/s CFP mechanical dimensions should be compliant with CFP MSA specification.

Detailed dimensions are shown in Figure 5.



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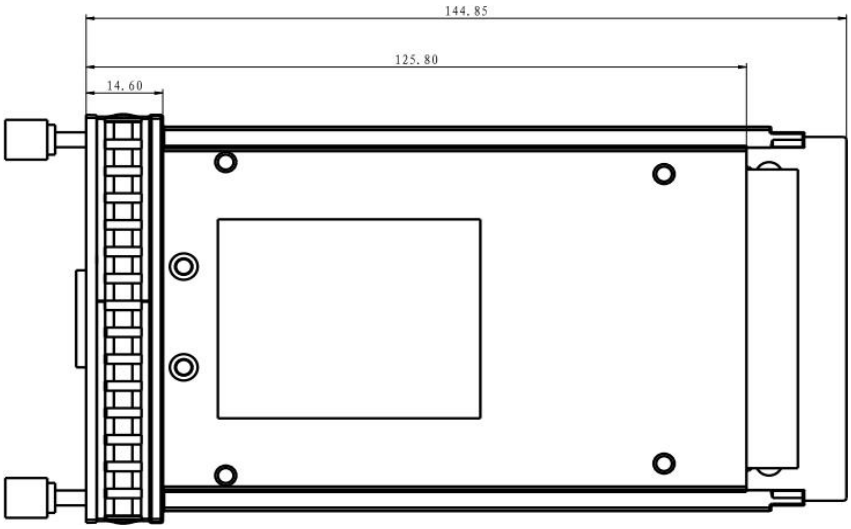

Figure 5. 100Gb/s CFP Mechanical Dimensions(unit:mm)

The mechanical dimensions of the electrical connectors on the CFP Host PCB are shown in Figure 6

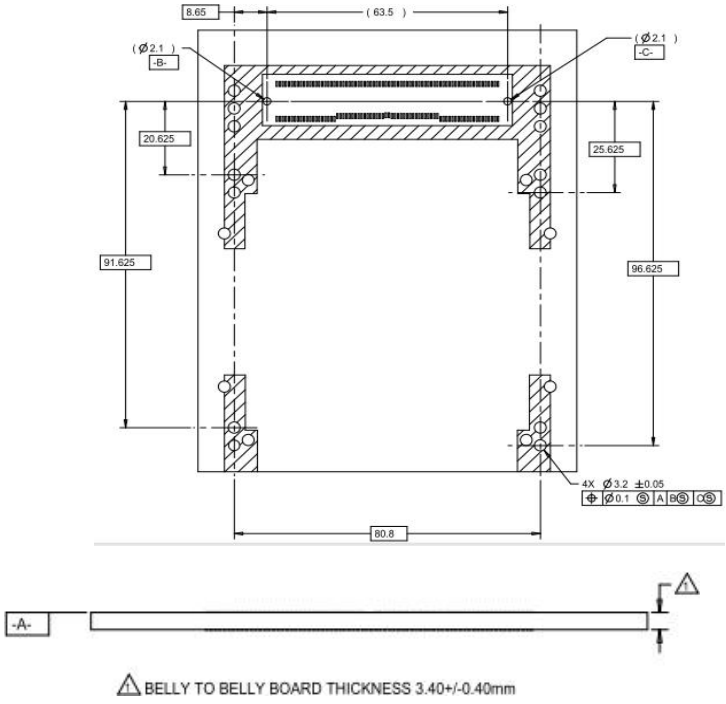

Figure 6 Mechanical Dimensions of Electrical Connectors on CFP Host PCB

● Warnings

Handling Precautions: This device is susceptible to damage as a result of electrostatic discharge (ESD). A static free environment is highly recommended. Follow guidelines according to proper ESD procedures.

Laser Safety: Radiation emitted by laser devices can be dangerous to human eyes. Avoid eye exposure to direct or indirect radiation.